

FEB 20 2003
PATENT & TRADEMARK OFFICE

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| U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY DOCKET NO. | SERIAL NO. |
| | 202887US2 | 09/778,104 |
| | APPLICANT | |
| | Yuuichi HIRANO, et al. | |
| LIST OF REFERENCES CITED BY APPLICANT | FILING DATE | GROUP |
| | February 7, 2001 | 2826 |

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE IF APPROPRIATE |
|---------------------|----|--------------------|------|------|-------|--------------|-------------------------------|
| | AA | | | | | | |
| | AB | | | | | | |
| | AC | | | | | | |
| | AD | | | | | | |
| | AE | | | | | | |
| | AF | | | | | | |
| | AG | | | | | | |
| | AH | | | | | | |
| | AI | | | | | | |
| | AJ | | | | | | |
| | AK | | | | | | |
| | AL | | | | | | |
| | AM | | | | | | |
| | AN | | | | | | |

FOREIGN PATENT DOCUMENTS

| | | DOCUMENT NUMBER | DATE | COUNTRY | TRANSLATION | |
|--|----|--------------------|------|---------|-------------|----|
| | | | | | YES | NO |
| | AO | | | | | |
| | AP | | | | | |
| | AQ | | | | | |
| | AR | | | | | |
| | AS | | | | | |
| | AT | | | | | |
| | AU | | | | | |
| | AV | | | | | |

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

| | | |
|------|----|--|
| VAMS | AW | Don Monroe, Jack Hergenrother, The Vertical Replacement Gate (VRG) Process for Scalable General-purpose Complementary Logic, Bell Labs, Lucent Technologies, Murray Hill, NJ |
| | AX | |
| | AY | |
| | AZ | |

☐ Additional References sheet(s) attached

Examiner

Victor A. Mandala Jr.

Date Considered 5-14-03

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.